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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SINGH, DALIP K	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/895,777	DOYLE ET AL.	
	Examiner	Art Unit	
	Dalip K Singh	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14,16-18 and 20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14,16-18 and 20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06-09-2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Request for Reconsideration

1. This Office Action is in response to applicant's request for reconsideration dated July 26, 2004 in response to PTO Office Action dated April 22, 2004.

2. Applicant's arguments filed July 26, 2004 have been fully considered and are not persuasive.

3. Regarding applicant's argument with respect to claim 1 that "Potter does not disclose a time allocator arbitrating the use of the graphics-rendering engine between two or more independent images", applicant's attention is drawn to col. 8, lines 25-35; lines 37-67 where Potter discloses that each attribute processor 314 includes its own dedicated back end unit 234; that timing buffer 248 is coupled with each of the back end units for delivering synchronized timing signals to each of the slave units 238 thus providing arbitration for two or more independent images. As far as amount of graphical data not being the same as two or more independent images, one cannot look at graphical data in segments and claim this now constitutes an image and now it not an image. The fact that graphical data is processed is sufficient to a person of ordinary skill in the art at the time invention was made to consider processing of graphical data to be equivalent to processing of image.

4. Regarding applicant's argument with respect to claim 17 that "Flurry does not disclose the concurrent rendering of instructions associated with multiple independent images within a first instruction-stream", applicant's attention is brought Flurry col. 7, lines 1-65 "...each entry in the domain array 70 contains a link to the device process...RCM 22 can authorize access to independent domains of display devices independently...a device domain is an environment within the device to which a graphics process is providing data...". Merely pointing to col. 5, lines 25-30 does not provide for a persuasive argument as col. 7, lines 1-65 describes concurrent rendering of instructions.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim(s) 1-3, 7-12, 17, 18 and 20-27 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,455,958 to Flurry et al. in view of U.S. Patent No. 6,157,393 to Potter et al.

a. Regarding claim(s) 1 and 24, Flurry et al. discloses a graphics-rendering engine (X Server program module 14, Fig. 1...as a display resource manager...col. 4, lines 14-44) to concurrently render two or more independent images for display on multiple display devices (...this invention is designed to function with several display devices connected to it...col. 5, lines 25-30) and a graphics context manager (rendering context manager (RCM) 22, Fig. 1) (...initially, Client B 18 and Client C 20,...access the X Server 14 in order to have display device resources...allocated to them...these accesses are performed in a manner that allows the client B 18 and Client C 20 to exist independently of each other...col. 4, lines 14-44...the rendering context manager (RCM) 22 is to ensure that as it permits each applications program to access the display device, it also places on the display device the proper rendering context, or environment , for that applications program...col. 5, lines 6-25) to store in a first memory area and restore from the first memory area information describing a first rendering context associated with the first independent image, the graphics context manager to store in a second memory area and restore from the second memory area information describing a second rendering context associated with the second independent image (...each entry in the domain array 70

contains a link to the device process...RCM 22 can authorize access to independent domains of display devices independently...a device domain is an environment within the device to which a graphics process is providing data...col. 7, lines 1-65). However, Flurry et al. **is silent about** time allocating to arbitrate the use of the graphics-rendering engine (X Server program module 14, Fig. 1...as a display resource manager...col. 4, lines 14-44) between the two or more independent images. Potter et al. **discloses** a time allocator (timing buffer 248) for graphics accelerator 200 (See Fig. 2C & 3A; col. 9, lines 58-67...these connections enable fractional amounts of data to be transmitted...col. 10, lines 7-23;...only fractional amounts of graphical data for pixels are received by the destination processor during each clock cycle...col. 2, lines 35-45) which suggests arbitrating the use of a graphics-rendering engine (...the graphics accelerator...includes a controller...causes...processor to produce...amount of graphical data during each clock cycle...col. 2, lines 60-65). Potter et al. further **discloses** programmability for usage of the graphics-rendering engine (...the first amount may be an odd number...the second amount may be calculated by rounding up...col. 2, lines 7-20). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Flurry et al. with the feature "a time allocator arbitrating the use of graphics-rendering engine between the two or more independent images" as taught by Potter et al. **because** it increases processing efficiency.

b. Regarding claim 2, Flurry et al. **discloses** as shown above a plurality of memory areas, each memory area to store a rendering context associated with the instructions from a particular graphics application;; and a plurality of context identification registers including a first context identification register and second context identification register, the first context identification register contains information to point to an address of the

first memory area, the second context identification register contains information to point to an address of the second memory area (...Fig. 3 is a flow chart...in step 700, the rendering context manager saves the user mode environment (such as...registers and the stack)...col. 6, lines 34-67).

c. Regarding claim 3, Flurry et al. **discloses** registers and saves the stack (Fig. 3). Flurry et al. **does not explicitly disclose** a third register to track which memory area in the plurality of memory areas contains the rendering context information to be supplied to the graphics-rendering engine. However, it would have been obvious to a person of ordinary skill in the art at the time invention was made to include such a register **because** it would improve the efficiency of rendering context manager.

d. Regarding claim 7, Flurry et al. **discloses** the first memory area to contain instructions for the two or more independent images in a first instruction stream (...the rendering context manager 22 provides...ensuring that only one of the processes wishing to access the display device...can do so at any given time, and...switching the display device rendering contexts required by the applications programs...col. 5, lines 6-24).

e. Regarding claim 8, it is similar in scope to claim 7 above and is rejected under the same rationale.

f. Regarding claim 9, it is similar in scope to claim 7 above and is rejected under the same rationale.

g. Regarding claim 10, Flurry et al. **discloses** a single display device 12 is connected to the RCM 22 (col. 5, lines 25-30).

h. Regarding claims 11 and 12, Flurry et al. **discloses** an instruction memory area (RCM common 50, Fig. 5); registers to define a start and an end to the instruction memory area (element 32, Fig. 2) and a memory access engine (RCM 22) to fetch and deliver the instructions from the instruction memory area (element 32) to the graphics-

rendering engine; and a third memory area (domain array 70, Fig. 5) that can be invoked from an instruction stream.

i. Regarding claim(s) 17 and 25, Flurry et al. **discloses** the concurrently rendering instructions (col. 5, lines 25-30); storage in a first memory area instruction for a first independent image; restoring from a second memory area instruction for a second independent image (...each entry in the domain array 70 contains a link to the device process...RCM 22 can authorize access to independent domains of display devices independently...a device domain is an environment within the device to which a graphics process is providing data...col. 7, lines 1-65). Flurry et al. **is silent** about switching the first rendering context to the second rendering context and using a volatile memory device to track which memory area in the plurality of memory areas contains the rendering context information to be supplied to a graphics-rendering engine. Potter et al. **discloses** the switching between a first and a second rendering context wherein graphical data is directed to a display device from a plurality of graphics processors (col. 1, lines 53-67) and further **discloses** a memory device (memory 204) for storing graphics request streams received from the plurality of processing units for processing the graphics request stream (col. 7, lines 1-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Flurry et al. with the feature "memory device containing rendering context information" as taught by Potter et al. **because** it provides for efficient processing of graphics data and improves efficiency (col. 7, lines 9-15).

j. Regarding claim 18, Flurry et al. **discloses** RCM setting up a timer for each domain and registers the timer handler with the kernel similar to the instant claim 3 where programmable elapsed period of time to use the graphics engine (col. 9, lines 20-30.

k. Regarding claim 20, Flurry et al. **discloses** displaying the multiple independent images on single display device (Fig. 1).

l. Regarding claim 21, it is similar in scope to claim 17 above and is rejected under the same rationale.

m. Regarding claim 22, it is similar in scope to claim 1 above and is rejected under the same rationale.

n. Regarding claim 23, Flurry et al. **discloses** a time allocator controlling the input to the graphics-rendering engine (Fig. 3).

o. Regarding claim 26, Flurry et al. as modified by Potter et al. **discloses** taking instructions in the instruction stream and using them for real-time periods of use of the graphics-rendering engine (...graphical data is forwarded to the display device...in a round robin manner...from each attribute processor...the master RAMDAC...receives...thirty-nine bits of data per common clock cycles...col. 13, lines 5-26).

p. Regarding claim 27, Flurry et al. **discloses** rendering context manager saving the user mode environment and then establishing the kernel environment and handles the system call 32 and further **discloses** system call direction, function to be executed, and any parameters necessary for that function thereby functioning similar to the tracking register as recited in the instant claim limitation (col. 6, lines 34-67).

7. Claim(s) 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,455,958 to Flurry et al. in view of U.S. Patent No. 6,157,393 to Potter et al. as applied to claim 1 above, and further in view of U.S. Patent No. 5,703,806 to Puar et al.

a. Regarding claim 4, Flurry-Potter et al. **does not disclose** a first memory area being located on the same chip containing the graphics-rendering engine. Puar et al. **discloses** a graphics controller function being integrated on the same chip as the

memory (col. 2, lines 58-67). It would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Flurry-Potter combination with the feature "memory and graphics-rendering engine on the same chip" as taught by Puar et al. **because** it provides for low power consumption, and low pin and package counts thus resulting in cost savings.

8. Claim(s) 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,455,958 to Flurry et al. in view of U.S. Patent No. 6,157,393 to Potter et al. as applied to claim 2 above, and further in view of U.S. Patent No. 6,311,204 to Mills.

a. Regarding claim 14, Flurry-Potter combination **fails to suggest** a plurality of registers having a plurality of fields wherein a first field that determines whether the first register participates in an arbitration process to use the graphics rendering engine and a second field to point to a memory allocation. Mills. **discloses** processing system with register-based process sharing. The acquire bit portion 352 (Fig. 9A) of the semaphore register 350 indicates other processes when it engages the drawing acceleration engine similar to the instant claim where a first field indicates whether the first register will participate in using the graphics engine (col. 27, lines 18-63). The process identifier portion 354 of the semaphore register 350 can be made to point to a memory location for fetching instructions from a first instruction stream. This is not explicitly discloses but such operation falls within the realm of fetching instructions being pointed to by a process identifier portion of the semaphore register. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Flurry-Potter combination with the feature "register-based process sharing" as taught by Mills **because** this would result in improved efficiency and reduce cost and complexity.

b. Regarding claim 16, wherein a first module directs the graphics-rendering engine to process instructions stored in a first memory having an address defined by information contained in the plurality of the fields, this is implicitly taught by Mills as described above (fetching instructions being pointed to by a process identifier portion of the semaphore register) (col. 27, lines 18-63).

9. Claim(s) 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,455,958 to Flurry et al. in view of U.S. Patent No. 6,157,393 to Potter et al. as applied to claim 2 above, and further in view of U.S. Patent No. 6,252,600 B1 to Kohli et al.

a. Regarding claim 5, Flurry et al. **does not disclose** a two dimensional and three dimensional image being processed. Kohli et al. **discloses** a graphics context management arrangement that involves two dimensional and three dimensional image processing (col. 4, lines 46-67; Fig. 3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Flurry et al. with the feature "two and three dimensional processes in a graphics context management" as taught by Kohli et al. **because** it provides for minimum pipeline latency associate with context switching (col. 2, lines 35-40).

c. Regarding claim 6, it is similar in scope to claim 5 above and is rejected under the same rationale.

Conclusion

10. Applicant's arguments have been considered but they are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(703) 305-3895**. The examiner can normally be reached on Mon-Thu (8:00AM-6: 30PM) Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(703) 308-6829**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

dks

November 3, 2004

Matthew C. Bella

MATTHEW C. BELLA
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